AVR081: Replacing AT90S4433 by ATmega8

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Introduction

This application note is a guide to assist current AT90S4433 users in converting existing designs to the ATmega8. ATmega8 contains more Flash, SRAM, and EEPROM memory space than AT90S4433, and it has additional peripheral modules and features. Still the pin-out of the two devices are identical, and with a few modifications to the I/O Register access, the ATmega8 can replace AT90S4433 on existing circuit boards. In addition to the functional changes, the electrical characteristics of the ATmega8 are different including an increase in operating frequency because of a change in process technology. Check the data sheet for detailed information.

AT90S4433 Errata Corrected in ATmega8

The following items from the Errata Sheets of the AT90S4433 do not apply to the ATmega8. Refer to the AT90S4433 Errata Sheet for a more detailed description of the Errata.

Fuses and Programming Mode

When programming the ATmega8 in Serial Programming mode, it is possible to program the Flash and EEPROM after programming the Fuses. If leaving Serial Programming mode, it is possible to re-enter Programming mode.

Incorrect Channel Changes in Free Running Mode

In ATmega8, the MUXn and REFS1:0 bits in the ADMUX Register are buffered through a temporary register to which the CPU has random access. This ensures that the channels and reference selection only takes place at a safe point during the conversion. Refer to the ATmega8 data sheet for further information and advices on how to change these registers in Free Running mode.

8-bit AVR® Microcontroller

Application Note

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Bandgap Reference Stabilizing Time

In ATmega8, the Bandgap Reference Voltage stabilizes within the time specified in the data sheet, independent from whether the internal Brown-out Detector is enabled or not.

Brown-out Detection Level

In ATmega8, the Brown-out Detection level is not influenced by activity on the I/O pins.

Serial Programming at Voltages Below 2.9V

There are no restrictions on the supply voltage or system frequency as long as the device is operated inside the voltage and frequency range specified in the data sheet for the ATmega8.

UART Looses Synchronization if RXD Line is Low when UART Receive is Disabled

The UART is replaced with a USART, which does not have this problem. The starting edge of a reception is only accepted as valid if the Receive Enable bit in the USART Control Register is set.

Differences in Pin-out

ATmega8 has alternate functions on some of its I/O pins that the AT90S4433 did not have. This will normally not create any problem when porting the code, as long as the alternate functions (which were not present in AT90S4433) are not used. The succeeding subsections discuss issues concerning the pin-out that the designer should consider when porting a design from AT90S4433 to ATmega8.

PC6 ($\overline{\text{RESET}}$)

AT90S4433 has a dedicated $\overline{\text{RESET}}$ pin, while ATmega8 has a pin that combines the $\overline{\text{RESET}}$ function with the I/O pin PC6. The I/O pin function is enabled by programming the RSTDISBL Fuse. Hence, make sure the RSTDISBL Fuse is unprogrammed when porting a design from AT90S4433.

PB7:6 (XTAL/TOSC)

AT90S4433 has dedicated pins for XTAL1 and XTAL2, while ATmega8 combines the I/O pin PB7 with XTAL2 and TOSC2, an the I/O pin PB6 with XTAL1 and TOSC1. Set the CKSEL Fuses to select either external crystal/ceramic resonator, external low frequency crystal, or external clock, and the pins will be dedicated to XTAL1 and XTAL2 only, as in AT90S4433.

ADC7:6

ATmega8 in TQFP (and MLF) package supports two ADC channels – ADC6 and ADC7– on pin 19 and pin 22 respectively. These pins are inputs only, and will not create trouble on a circuit board when replacing AT90S4433, as this device has No Connect on these pins.

V_{CC}/GND

ATmega8 in TQFP (and MLF) package supports an additional pair of power pins; GND on pin three and V_{CC} on pin six. These pins where No Connect on AT90S4433. These pins need not be connected if the ATmega8 directly replaces a AT90S4433 on a circuit board, but the user is advised to use it on new designs, as the extra power pins improve noise immunity.

Changes to Names

The following control bits have changed names, but have the same functionality and placement when accessed as in AT90S4433:

Table 1. Changed Bit Names

Bit Name in AT90S4433	Bit Name in ATmega8	I/O Register (AT90S4433)	Comments
PWM10	WGM1n0	TCCR1A	
PWM11	WGM1n1	TCCR1A	
CTC1	WGM12	TCCR1B	
CHR9	UCSZ2	USCRB	
OR	DOR	UCSRA	
OCIE1	OCIE1A	TIMSK	Bit position is changed. See “Bit positions in TIMSK and TIFR” on page 5.
OCF1	OCF1A	TIFR	Bit position is changed. See “Bit positions in TIMSK and TIFR” on page 5.
WDTOE	WDCE	WDTCR	Not directly compatible. See “Changes to Watchdog Timer” on page 10.
AINBG	ACBG	ACSR	

The following I/O Registers have changed names, but include the same functionality and placement when accessed as in AT90S4433:

Table 2. Changed Register Names

Register name in AT90S4433	Register name in ATmega8	Comments
EEAR	EEARL	Due to larger memory size the EEAR is expanded to 16-bit.
(EEAR)	EEARH	
SP	SPL	Due to larger memory size the SP is expanded to 16-bit.
(SP)	SPH	
GIMSK	GICR	
MCUSR	MCUCSR	
UBRRHI	UBRRH	Register has changed I/O address. See “Improvements to SPI and USART” on page 8.

The interrupt vector table of the ATmega8 differs from the one of AT90S4433. The differences are listed in Table 3.

Table 3. Changes to Interrupt Vectors[1]

Vector No.	Program Address	AT90S4433	ATmega8
1	$000	RESET	RESET
2	$001	INT0	INT0
3	$002	INT1	INT1
4	$003	**TIMER1 CAPT**	**TIMER2 COMP**
5	$004	**TIMER1 COMP**	**TIMER2 OVF**
6	$005	**TIMER1 OVF**	**TIMER1 CAPT**
7	$006	**TIMER0 OVF**	**TIMER1 COMPA**
8	$007	**SPI, STC**	**TIMER1 COMPB**
9	$008	**UART, RX**	**TIMER1 OVF**
10	$009	**UART, UDRE**	**TIMER0 OVF**
11	$00A	**UART, TX**	**SPI, STC**
12	$00B	**ADC**	**USART, RXC**
13	$00C	**EE_RDY**	**USART, UDRE**
14	$00D	**ANA_COMP**	**USART, TXC**
15	0x00E		**ADC**
16	0x00F		**EE_RDY**
17	0x010		**ANA_COMP**
18	0x011		**TWI**
19	0x012		**SPM_RDY**

Note: 1. Discrepancies are marked with bold face.

Improvements to Timer/Counters and Prescalers

For details about the improved and additional features, please refer to the data sheet. The following features have been added:

- The Prescalers in ATmega8 can be reset.
- Variable top value in PWM mode.
- For Timer/Counter1, Phase and Frequency Correct PWM mode in addition to the Phase Correct PWM mode (also in Timer/Counter2).
- Fast PWM mode.

Differences Between ATmega8 and AT90S4433

Most of the improvements and changes apply to all the Timer/Counters and the description below is written in a general form. A lower case “x” replaces the output channel (A or B for Timer/Counter1, N/A for Timer/Counter0), while “n” replaces the Timer/Counter number (n = 0 or 1). Timer/Counter2 is not present in AT90S4433.

Bit positions in TIMSK and TIFR

All interrupt masks and flags in AT90S4433 are present in ATmega8, but not in the same positions. Table 4 shows the correspondence between bit positions in AT90S4433 and bit positions in ATmega8 regarding the TIMSK and TIFR Registers.

Table 4. Bit Positions in TIMSK and TIFR

TIMSK	TIFR	AT90S4433 Bit Position	ATmega8 Bit Position
TOIE1	TOV1	7	2
OC1E1	OCF1	6	4
TCIE1	ICF1	3	5
TOIE0	TOV0	1	0

TCNT1 Cleared in PWM Mode

In AT90S4433 there are three different PWM resolutions – 8, 9, or 10 bits. Though only 8, 9, or 10 bits are compared, it is still possible to write values into the TCNT1 Register that exceed the resolution. Thus, the Timer/Counter has to complete the count to 0xFFFF before the reduced resolution becomes effective (i.e, if 8-bit resolution is selected and the TCNT1 Register contains 0x0100, the top value (0x00FF) will not be effective until the counter has counted up to 0xFFFF, turned, and counted down to 0x0000 again). In ATmega8 this has been changed so that the unused bits in TCNT1 are being cleared to zero to avoid this unintended counting up to 0xFFFF. In the ATmega8, the TCNT1 Register never exceeds the selected resolution.

ATmega8

The most significant bits in the TCNT1 Register will be cleared at the first positive edge of the prescaled clock.

- 8-bit PWM: TCNT1H7:0 = 0
- 9-bit PWM: TCNT1H7:1 = 0
- 10-bit PWM: TCNT1H7:2 = 0

AT90S4433:

TCNT1H not cleared.

OCR1xH Cleared in PWM Mode

Clearing OCR1xH in PWM mode is slightly different from clearing TCNT1. The AT90S4433 clears the six most significant bits if 8, 9, or 10 bits PWM mode is selected. Hence, if 0xFFFF is written to OCR1x in PWM mode and OCR1x is read back, the result is 0x03FF regardless of which PWM mode that is selected. In ATmega8 the number of cleared bits depends on the resolution.

ATmega8

The most significant bits in OCR1AH are cleared when they are updated at the TOP value of the counter.

- 8-bit PWM: OCR1xH7:0 = 0
- 9-bit PWM: OCR1xH7:1 = 0
- 10-bit PWM: OCR1xH7:2 = 0

AT90S4433

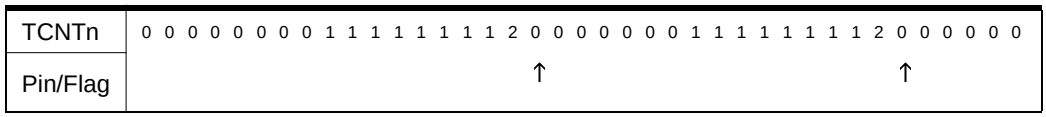
The six most significant bits in the OCR1H are cleared regardless of the resolution.

Clear Timer/Counter1 on Compare Match with Prescaler

The relation between a Clear on Compare match and the internal counting of the Timer/Counters has been changed. The Clear on Compare match in the AT90S4433 clears the Timer/Counter after the first internal count matching the compare value, whereas the ATmega8 clears Timer/Counter after the last internal count matching the compare value. See Figure 1 and Figure 2 for details on clearing, flag setting, and pin change.

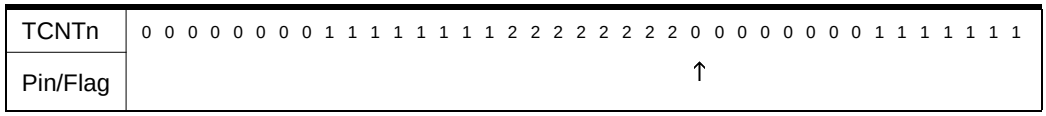
Example: OCR1x = 0x02 when prescaler is enabled (divide clock by eight).

Figure 1. Setting Output Compare Flag/Pin for AT90S4433[1]



Note: 1. "↑" Indicates where the Output Compare Flag/Pin will be set.

Figure 2. Setting Output Compare Flag/Pin for ATmega8[1]



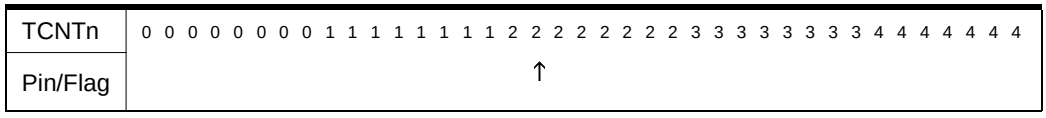
Note: 1. "↑" Indicates where the Output Compare Flag/Pin will be set.

Setting of Output Compare Pin/Flag with Prescaler Enabled (Applies to all Timer/Counters)

The relation between an Output Compare and the internal counting of the Timer/Counter has been changed. Output Compare in the AT90S4433 sets the Output Compare pin/flag after the first internal count matching the compare value, whereas the ATmega8 sets the Output Compare pin/flag after the last internal count matching the compare value. See Figure 3 and Figure 4 for details on Output Compare Flag setting and pin change.

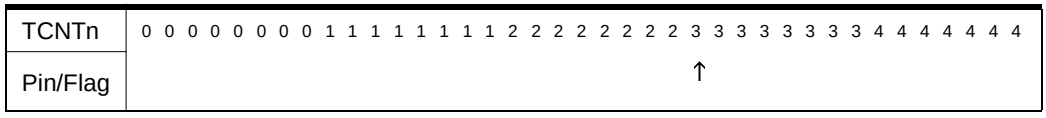
Example: OCR1x = 0x02, prescaler enabled (divide clock by 8)

Figure 3. Setting Output Compare Flag/Pin for AT90S4433[1]



Note: 1. "↑" Indicates where the Output Compare Flag/Pin will be set.

Figure 4. Setting Output Compare Flag/Pin for ATmega8[1]



Note: 1. "↑" Indicates where the Output Compare Flag/Pin will be set.

Write to OCR1x in PWM Mode, Change to Normal Mode Before OCR1x is Updated at the Top, Read OCR1

As described in the data sheet, the OCR1x Registers are updated at the top value when written. Thus, when writing the OCR1x in PWM mode, the value is stored in a temporary buffer. When the Timer/Counter1 reaches the top, the temporary buffer is transferred to the actual Output Compare Register. If PWM mode is left after the temporary buffer is written, but before the actual Output Compare Register is updated, the behavior differs between ATmega8 and AT90S4433.

ATmega8

If the OCR1x Register is read before the update is done, the actual compare value is read – not the temporary OCR1 buffer.

AT90S4433

If the OCR1A Register is read before the update is done, the value in the OCR1A buffer is read. For example, the value read is the one last written (to the OCR1A buffer), but since the Timer/Counter never reached the top value, it was not latched into the OCR1A Register. Hence, the value that is used for comparison is not necessarily the same as being read.

Note: This applies to 16-bit Timer/Counter only, for 8-bit Timer/Counter2 in ATmega8, the temporary buffer is read.

Memory of Previous OCnx pin Level

In AT90S4433, there are two settings of COMnx1:0 that do not update the OCnx pin in PWM mode (0b00 and 0b01), and one setting of COMnx1:0 in non-PWM mode (0b00). Assume the Timer/Counter is taken from a state that updates the OCnx pin to a state that does not, and then back again to a state that does update the OCnx pin. The following differences should be noted:

ATmega8

The level of the OCnx pin before disabling the Output Compare mode is remembered. Re-enabling the Output Compare mode will cause the OCnx pin to resume operation from the state it had when it was disabled. All Output Compare pins are initialized to zero on Reset.

AT90S4433

For Timer/Counter1 in non-PWM mode, a compare match during the time when the Timer/Counter is not connected to the pin will reset the OC1 pin to the low level once enabled again. PWM mode will update the Internal Register for the OC1 pin, such that the state of the pin is unknown once enabled again.

Changes to ADC

The ADC in ATmega8 has been improved by:

- ATmega8 supports both left adjusted and right adjusted 10-bit results.
- Two extra ADC channels (MLF and TQFP packages only).

It should be noted that the input channels ADC4 and ADC5 have less accuracy than the other ADC channels in ATmega8. This is due to these pins being shared by the Two-wire Interface, and hence internally powered from the digital power pins V_{CC}, not AVCC. This is not the case for AT90S4433. Please consult the Electrical Characteristics section of the data sheet for information regarding accuracy of the ADC channels.

The ADCBG bit in the ADMUX Register selects a bandgap reference as input to the ADC in AT90S4433. The same thing is obtained in ATmega8 by setting MUX3:0 = 0b1110. The REFS1:0 bits replaces the bit position for ADCBG and an unused position in AT90S4433. These bits determines the reference voltage, and have nothing to do with the input to the ADC.

Changes to Power Management

ATmega8 contains more sleep modes than AT90S4433. This means that the SM bit in AT90S4433 is extended to SM2:0 in ATmega8. SM = “0” in AT90S4433 corresponds to SM2:0 = 0b000 in ATmega8, and SM = “1” in AT90S4433 corresponds to SM2:0 = 0b010 in ATmega8.

Be aware that EEPROM write access must be completed before entering power down sleep mode. Otherwise the system oscillator will continue to run, drawing additional current.

Important: The bit position for SE is changed from AT90S4433 to ATmega8. See data sheet for ATmega8 for a description of bit positions for SE, SM2, SM1, SM0, and the additional sleep modes.

Improvements to SPI and USART

Both SPI and USART have new Double Speed modes which allow higher communication speed.

The UART in AT90S4433 has been replaced by a USART in ATmega8. The ATmega8 USART is compatible with the AT90S4433 UART with one exception: The two-level Receive Register acts as a FIFO. The following must be kept in mind:

- A second buffer register has been added. The two buffer registers operate as a circular FIFO buffer. Therefore the UDR must only be read once for each incoming data. More important is the fact that the Error Flags (FE and DOR) and the ninth data bit (RXB8) are buffered with the data in the receive buffer. Therefore the status bits must always be read before the UDR Register is read. Otherwise the error status will be lost since the buffer state is lost.
- The Receiver Shift Register can now act as a third buffer level. This is done by allowing the received data to remain in the Serial Shift Register if the buffer registers are full, until a new start bit is detected. The USART is therefore more resistant to Data OverRun (DOR) error conditions.

The UBRRHI Register has address 0x3 (0x23) in AT90S4433. In ATmega8, this register is moved to address 0x20 (0x40), and the URSEL bit selects between accessing the UBRRH or the UCSRC Register at this address. Write the URSEL bit to zero when writing data to the UBRRH Register.

Another minor difference is the initial value of RXB8, which is “1” in the UART in AT90S4433 and “0” in the USART in ATmega8

Changes to EEPROM Write Timing

In AT90S4433, the EEPROM write time is dependent on supply voltage, typically 2.5 ms @ V_{CC} = 5V and 4 ms @ V_{CC} = 2.7V. In ATmega8, the EEPROM write time takes 8,448 cycles of the calibrated RC Oscillator (regardless of the clock source and frequency for the system clock). The calibrated RC Oscillator is assumed to be calibrated to 1.0 MHz regardless of V_{CC}, i.e., typical write time is 8.4 ms.

Note: Changing the value in the OSCCAL Register affects the frequency of the calibrated RC Oscillator and hence the EEPROM write time.

Programming Interface

Some changes have been done to the programming interface, especially in the In-System Programming interface. This has been done to support all the additional fuses in ATmega8. The timing requirements are unchanged. See the ATmega8 data sheet for details.

The Parallel Programming algorithm is changed. The most significant change is the introduction of the PAGEL pin on PD7 and the BS2 pin on PA0. This extension is needed to support page programming of Flash, EEPROM, and additional fuses in ATmega8. Note that the additional fuses and Lock bits also require a change in the fuse writing algorithm. The timing requirements for parallel programming have been changed. See the ATmega8 data sheet for details.

The STK500 supports both In-System Programming and parallel programming of the ATmega8.

Fuse Settings

ATmega8 contains more fuses than AT90S4433. Table 5 shows the AT90S4433 compatible Fuse settings. Some of the Fuses are described further in the following sections.

Table 5. Comparing Fuses in AT90S4433 and ATmega8

Fuse	Default AT90S4433 Setting	Default ATmega8 Setting	AT90S4433 Compatible Setting
RSTDISBL	–	1	1
WDTON	–	1	1 (2)
SPIEN	0	0	0
CKOPT	–	1	0 (3)
EESAVE	–	1	1
BOOTSZ1	–	0	0 (N/A) (4)
BOOTSZ0	–	0	0 (N/A) (4)
BOOTRST	–	1	1
BODLEVEL	1	1	1
BODEN	1	1	1
SUT1	–	1	See note (5)
SUT0	–	0	See note (5)
CKSEL3	–	0	See note (5)
CKSEL2	0	0	See note (5)
CKSEL1	1	0	See note (5)
CKSEL0	0	1	See note (5)

Notes:
1. A dash indicates that the Fuse is not present in AT90S4433.
2. See “Changes to Watchdog Timer” on page 10.
3. See “Oscillators and Selecting Start-up Delays” on page 10.
4. SPM and Self-Programming is not available in AT90S4433. The default factory setting of BOOTSZ1:0 is OK when porting the design to ATmega8.
5. The SUT and CKSEL setting must be considered when moving to ATmega8. See “Oscillators and Selecting Start-up Delays” on page 10.

Oscillators and Selecting Start-up Delays

ATmega8 provides more Oscillators and Start-up Time selections than AT90S4433. During wake-up from Power-down mode, the ATmega8 uses the CPU frequency to determine the duration of the wake-up delay, while AT90S4433 determines the delay from the WDT Oscillator frequency.

Follow the guidelines from the section “System Clock and Clock Options” in the ATmega8 data sheet to find appropriate start-up values.

Special attention must be paid when changing the fuses in In-System Programming mode. In-System Programming is dependent on a system clock. If wrong Oscillator setting is programmed, it may be impossible to re-enter In-System Programming mode due to missing system clock (Parallel Programming mode must then be used).

The crystal Oscillator in AT90S4433 is capable of driving an addition clock buffer from the XTAL2 output. In ATmega8, this is only possible when the CKOPT Fuse is programmed. In this mode the Oscillator has a rail-to-rail swing at the output, but at the expense of higher power consumption. Hence, do only program this fuse when rail-to-rail swing is required.

Changes to Watchdog Timer

The Watchdog Timer in ATmega8 is improved compared to the one in AT90S4433. In AT90S4433, the Watchdog Timer is either enabled or disabled, while ATmega8 supports two safety levels selected by the WDTON Fuse. Figure 6 summarizes the behavior for the two devices with regard to initial state, how to disable it, and how to change the Time-out of the Watchdog Timer.

Table 6. WDT Configuration in AT90S4433 and ATmega8.

Device	WDTON	Safety Level	WDT Initial State	How to Disable the WDT	How to Change Time-out
AT90S4433	N/A	N/A	Disabled	Timed sequence	No restriction
ATmega8	Unprogrammed	1	Disabled	Timed sequence	Timed sequence
ATmega8	Programmed	2	Enabled	Always enabled	Timed sequence

It can be seen that none of the safety levels in ATmega8 exactly matches the behavior of AT90S4433. By using safety level 1, the only difference is the need for a timed sequence for changing Time-out.

The frequency of the Watchdog Oscillator in ATmega8 is close to 1.0 MHz for all supply voltages. The typical frequency of the Watchdog Oscillator in AT90S4433 is close to 1.0 MHz at 5V, but the Time-out period increases with decreasing V_{CC}. This means that the selection of Time-out period for the Watchdog Timer (in terms of number of WDT Oscillator cycles) must be reconsidered when porting the design to ATmega8. Refer to the data sheet for ATmega8 for further information.

Other Concerns

The ATmega8 has a Signature Byte different from the one used in AT90S4433. Make sure you are using the Signature Byte of ATmega8 when porting the design.

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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